NMAM INSTITUTE OF TECHNOLOGY, NITTE

Off-Campus Centre of Nitte (Deemed to be University)

First Semester B.Tech. (CBCS) Degree Examinations

December 2022

EC1002-1 – APPLIED DIGITAL LOGIC DESIGN

Duration: 3 Hours | Max. Marks: 100

Note:

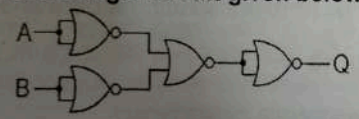
*Part – A: Multiple Choice Questions: Answer all **Twenty** questions in the **OMR Sheet** provided. Each question carries equal marks.*

*Part – B: Descriptive Answer type Questions: Answer **Five full** questions choosing **Two full** questions from **Unit – I & Unit – II each** and **One full** question from **Unit – III.***

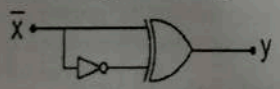
PART - A: MULTIPLE CHOICE QUESTIONS

20 Marks

1. **If we add an inverter at the output of AND gate, what function is produced?**
   A) XOR B) NAND C) OR D) NOR
2. **OR gate and _____ will form the NOR gate?**
   A) OR B) NAND C) AND D) NOT
3. **What are the canonical forms of Boolean expressions?**
   A) OR and XOR B) NOR and XNOR C) MAX and MIN D) SOP and POS
4. **The Boolean expression AB+AC'+BC simplifies to**
   A) BC+AC' B) AB+AC'+B C) AB+AC' D) AB+BC
5. **The output of the logic circuit given below represents _____ gate**



   A) OR B) NOR C) AND D) NAND
6. **The output Y of the logic circuit given below is:**



   A) 1 B) 0 C) X D) X'
7. **The minimum number of NAND gates required to realise AB+AB'C+AB'C' is**
   A) 3 B) 2 C) 1 D) 0
8. **_____ are universal logic gates**
   A) NAND and NOR B) NOR AND EX-OR C) AND and NOT D) OR and EX-OR
9. **One operation that is not given by magnitude comparator is**
   A) Equal B) Less than C) Greater than D) Sum
10. **Adding 1001 and 0010 gives the output of**
    A) 1011 B) 1111 C) 1010 D) 0000
11. **Major difference between half-adders and full-adders is**
    A) Full-adders are made up of two half-adders B) Full-adders can handle double digit numbers C) Full-adders have carry input capability D) None of these

12. **Binary subtraction of 0-1 yields**
A) Difference = 0, borrow = 0 B) Difference = 1, borrow = 0
C) Difference = 1, borrow = 1 D) Difference = 0, borrow = 1

13. **How many basic binary subtraction operations are possible?**
A) 1 B) 4
C) 3 D) 2

14. **What are the two types of basic adder circuits?**
A) Sum and carry B) Half-adder and full-adder
C) Asynchronous and synchronous D) One and two's-complement

15. **Which of the following is correct for full adders?**
A) Full adders have the capability of directly adding decimal numbers B) Full adders are used to make half adders
C) Full adders are limited to two inputs since there are only two binary digits D) In a parallel full adder, the first stage may be a half adder

16. **If A and B are the inputs of a half adder, the sum is given by ____**
A) A AND B B) A OR B
C) A XOR B D) A EX-NOR B

17. **The characteristic equation for S-R flip flop is**
A) $\bar{S} + \bar{R}Q$ B) $\bar{S} + R\bar{Q}$
C) $S + \bar{R}Q$ D) $S + RQ$

18. **Which of the following statements are TRUE regarding shift registers?**
A) A shift register is a group of flip flops B) It is not used for data storage
C) It is not used for the data movement D) Shift register includes set of latches

19. **The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____.**
A) 01110 B) 00001
C) 00101 D) 10101

20. **The minimum number of flip-flops that can be used to construct a modulus-5 counter is ____**
A) 3 B) 8
C) 5 D) 10

PART - B: DESCRIPTIVE ANSWER QUESTIONS

Unit – I

		Marks	BT*	CO*	PO*
1. a)	Perform number conversion of the given numbers. i) $345_{10} = (?)_2$ ii) $10110.011_2 = (?)_{16}$ iii) $AB24.C5_{16} = (?)_{10}$	5	L3	1	1
b)	Implement the given function using basic gates, NAND only and NOR only. Y=f(a, b, c) = a+b'+bc	5	L3	2	1
c)	Design a combinational circuit having four inputs (a, b, c, d) and one output (Y). Indicate logic 1at the output when majority of its inputs are logic 1, indicate logic 0 when majority of its input are logic 0. Output is not specified when number of 1's and 0's, are equal at the input.	6	L3	2	1
2. a)	Design a combinational logic circuit with inputs P, Q, R so that output S is high whenever P is zero or whenever Q=R=1.	5	L3	2	1
b)	State and prove the DeMorgan's laws using truth table method.	5	L2	1	1
c)	Find the minimal sum expression for the given Boolean function using QM technique. W=$f(a,b,c,d)= \Sigma m(0,1,2,3,6,7,8,9,14,15)$	6	L3	2	1
3. a)	Obtain minimal sum expression for the given Boolean functions using K-map method. i) P=$f(a,b,c,d)= \Sigma m(0,1,2,3,8,9)$ ii) Q=$f(a,b,c,d)= \Sigma m(0,1,2,3,6,7,8,9,14,15)$ iii) R=$f(a,b,c,d)= \Pi M(1,2,3,4,9,10)+dc(0,14,15)$.	5	L3	2	1

	b)	Convert the following equations into their Canonical forms. i) $R = L + \bar{M}(\bar{N}M + \bar{M}L)$ into SOP form, ii) $P = (\bar{w} + x)(y + \bar{z})$ into POS form.				
	c)	Design a combinational circuit which accepts two, 2-bit binary numbers and generates three outputs. The first output indicates logic 1 whenever the 2 numbers differ by 2 or more, the second output indicates logic 1 whenever the 2 numbers are identical, and the third output indicates logic 1 when the first number exceeds second number.	5	L3	1	1
			6	L3	2	1
		Unit – II				
4.	a)	Explain the operation of Master Slave JK flip flop with truth table and timing diagram. Write the symbol for the same.	5	L2	4	1
	b)	Implement Y=f(a,b,c)=∑m(1,4,5,7) using i) 8:1 MUX ii) 4:1 MUX using a and b as select lines.	5	L3	3	1
	c)	Design a combinational logic circuit to compare two 2-bit numbers.	6	L3	3	1
5.	a)	Implement the given functions using decoder with minimum number of gate inputs. i) F1 = f(a,b) =∑m(0,1,3) ii) F2 = f(a,b,c) = ∑m(0,2,3,5,7) iii) F3 = f(a,b,c) = ∏M(1,2,3,5,6,7).	5	L3	3	1
	b)	Explain 4-bit parallel subtractor with necessary block diagram.	5	L2	3	1
	c)	Explain the working of +ve edge triggered D flip flop with relevant logic diagram, function table and timing diagram.	6	L2	4	1
6.	a)	Design 8:3 line encoder with relevant truth table, output expressions and draw the logic diagram using basic gates.	5	L2	3	1
	b)	Convert JK flip to SR and T flip flop.	5	L2	4	1
	c)	Design a common cathode BCD to seven segment decoder.	6	L3	3	1
		Unit – III				
7.	a)	Explain the working of 4-bit ripple down counter with relevant diagram and function table.	8	L2	5	1
	b)	Explain the working of following shift registers with relevant block diagram and appropriate examples. i) 4-bit serial in serial out, ii) 4-bit parallel in parallel out, iii) 4-bit serial in parallel out.	8	L2	5	1
8.	a)	Derive characteristic equations of JK, SR and T flip flops.	8	L2	5	1
	b)	Design a synchronous counter to count 0→1→4→6→7→5→0 using positive edge triggered JK flip flops with minimal combinational gating.	8	L3	5	1

BT* Bloom's Taxonomy, L* Level; CO* Course Outcome; PO* Program Outcome

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